CLAIMS

1. A memory module, comprising:
   a. a memory cell having a memory state; and
   b. a local sense amplifier coupled with the memory cell, the local sense amplifier sensing the memory state and producing a local memory state signal representative thereof, wherein the local sense amplifier produces a limited swing voltage signal.

2. The memory module of Claim 1, further comprising a global sense amplifier, coupled with the local sense amplifier, the global sense amplifier sensing the local memory state signal and producing a global memory state signal representative thereof.

3. The memory module of Claim 1, further comprising a plurality of memory cells coupled with the local sense amplifier.

4. The memory module of claim 3, further comprising:
   a. a plurality of local sense amplifiers; and
   b. a global sense amplifier, coupled with the plurality of local sense amplifiers, a selected one of the plurality of local sense amplifiers sensing the memory state and producing a local memory state signal representative thereof, the global sense amplifier sensing the local memory state signal and producing a global memory state signal representative thereof, and wherein the plurality of memory cells coupled with the global sense amplifier is disposed as a memory column.

5. The memory module of Claim 3, wherein the plurality of memory cells comprises a memory cell subcolumn, and the local sense amplifier is coupled with a single memory cell subcolumn.

6. The memory module of Claim 3, wherein the plurality of memory cells is partitioned to form a plurality of memory cell subcolumns each having a respective plurality of memory cells, and the local sense amplifier is coupled with the plurality of memory cell subcolumns.

7. The memory module of Claim 4, further comprising a plurality of global sense amplifiers, selected ones of the plurality of global sense amplifiers having a respective plurality of local sense amplifiers coupled therewith, and selected ones of the plurality of local sense amplifiers being coupled with a respective plurality of memory cells, selected others of the plurality of global sense amplifiers being coupled with the selected ones such that the selected ones of the plurality of global sense amplifiers are local sense amplifiers relative to the selected others of the plurality of global sense amplifiers, each local sense amplifier producing a respective local memory state signal to which a corresponding global sense amplifier is responsive.

8. The memory module of Claim 1, wherein the local sense amplifier is responsive to a limited swing voltage signal from the memory cell representative of the memory state.

9. The memory module of Claim 2, wherein the global sense amplifier is responsive to a limited swing voltage signal representative of the memory state.

10. The memory module of Claim 8, wherein the global sense amplifier produces a limited swing voltage signal representative of the memory state.

11. The memory module of Claim 3, wherein one of the local sense amplifier is responsive to a limited swing voltage signal from the memory cell representative of the memory state.

12. The memory module of Claim 4, wherein one of the local memory state signal and the global memory state signal is a limited swing voltage signal.

13. The memory module of Claim 12, wherein both of the local memory state signal and the global memory state signal is a limited swing voltage signal.

14. The memory module of Claim 1, further comprising a local wordline decoder coupled with the memory cell, the local wordline decoder selecting the memory cell responsive to a local selection signal.

15. The memory module of Claim 2, further comprising a local wordline decoder coupled with the memory cell, the local wordline decoder selecting the memory cell responsive to a local selection signal.

16. The memory module of Claim 15, further comprising a global wordline decoder coupled with the local wordline decoder, the global wordline decoder producing the local selection signal responsive to a global selection signal.

17. The memory module of Claim 4, further comprising a plurality of local wordline decoders coupled with respective memory cells, a selected one of the plurality of local wordline decoders selecting one of the respective memory cells responsive to a local selection signal.

18. The memory module of Claim 17, further comprising a global wordline decoder coupled with the plurality of local wordline decoders, the global wordline decoder producing the local selection signal responsive to a global selection signal, and wherein the plurality of memory cells coupled with the global wordline decoder is disposed as a memory row.

19. The memory module of Claim 18, further comprising a plurality of global wordline decoders each coupled with a corresponding plurality of local wordline decoders, a selected one of the plurality of global wordline decoders producing a local selection signal responsive to a global selection signal.

20. The memory module of Claim 7, further comprising a plurality of local wordline decoders coupled with respective memory cells, selected ones of the plurality of local wordline decoders selecting respective memory cells responsive to a corresponding local selection signal.

21. The memory module of Claim 20, further comprising a global wordline decoder coupled with the plurality of local wordline decoders, the global wordline decoder producing the local selection signal responsive to a global selection signal, and wherein the plurality of memory cells coupled

with the global wordline decoder is disposed as a memory row.

22. The memory module of Claim 21, further comprising a plurality of global wordline decoders, selected ones of the plurality of global wordline decoders being coupled with a respective plurality of local wordline decoders, selected ones of the plurality of local wordline decoders being coupled with a respective plurality of memory cells, selected others of the plurality of global wordline decoders being coupled with the selected ones such that the selected ones are local wordline decoders relative to the selected others, each global wordline decoder producing a respective global selection signal to which the corresponding plurality of local wordline decoders is responsive.

23. The memory module of Claim 22, wherein one of the local memory state signal, the global memory state signal, the local selection signal, the global selection signal, and a combination thereof, comprises a limited swing voltage signal.

24. The memory module of Claim 22, wherein at least one of the global sense amplifier and the plurality of local sense amplifiers comprises one of a single-ended sense amplifier having sample-and-hold reference, and a charge-share limited-swing-driver sense amplifier.

25. The memory module of Claim 22, further comprising a wordline decoder having a first memory row and a second memory row coupled therewith, the wordline decoder decoding the first memory row, and being disposed to select and

decode the second memory row responsive to an alternative-row-select signal.

26. The memory module of Claim 22, further comprising:
    a. a redundant memory row; and
    b. a wordline decoder coupled an assigned memory row and the redundant memory row, the row decoder decoding the assigned memory row, and being disposed to select and decode the redundant memory row responsive to a redundant-row-select signal.

27. The memory module of Claim 22, wherein one of the plurality of global wordline decoders and local wordline decoders comprises an asynchronously-resettable row decoder.

28. The memory module of Claim 27, wherein the asynchronously-resettable row decoder has a first memory row and a second memory row coupled therewith, the row decoder decoding the first memory row, and being disposed to select and decode the second memory row responsive to an alternative-row-select signal.

29. The memory module of Claim 22, having a designated group of memory cells assigned to represent a logical portion of the memory structure, the structure further comprising:
    a. a redundant group of memory cells; and
    b. a redundancy controller coupled with the designated group and the redundant group, the redundancy controller assigning the redundant group to the logical portion of the memory structure, responsive to a preselected memory group condition.

30. The memory module of Claim 29, wherein the redundancy controller comprises a redundancy decoder responsive to an encoded signal representative of the preselected memory group condition.

31. The memory module of Claim 30, wherein the redundancy controller further comprises a plurality of selectable switches, the plurality of selectable switches encoding the preselected memory group condition.

32. The memory module of Claim 31, wherein the plurality of selectable switches are fuses.

33. The memory module of Claim 31, wherein the preselected memory group condition is a "FAILED" memory group condition, representative of a designated group malfunction.

34. The memory module of Claim 29, wherein each of the designated group and the redundant group comprises one of a memory row, a memory column, a preselected portion of a memory module, a selectable portion of a memory module, a memory module, and a combination thereof.

35. The memory module of Claim 25, wherein the wordline decoder includes a selection signal input, and further comprises comprises a multiplexer operably coupled with the first memory row and the second memory row, the multiplexer selectably directing the local selection signal from the wordline decoder selection signal input to the selected one of the first memory row and the second memory row.

36. The memory module of Claim 1, wherein the local sense amplifier comprises a high-precision delay measurement circuit.

37. The memory module of Claim 12, further comprising a high-precision delay measurement circuit constraining the limited voltage swing signal.

38. The memory module of Claim 37, wherein the high-precision delay measurement circuit comprises a ring oscillator executing oscillation cycle in a predefined oscillation period.

39. The memory module of Claim 38, wherein the ring oscillator executes a plurality of oscillation cycles by circulating an oscillation signal therein, and the ring oscillator comprises:

a. a plurality of oscillator stages; and

b. a plurality of oscillation signal detectors interposed between selected ones of the oscillator stages, the plurality of oscillation signal detectors detecting the location of the oscillation signal within the ring oscillator during a measured oscillation cycle, responsive to a measurement signal.

40. The memory module of Claim 39, wherein the high-precision delay measurement circuit further comprises a counter coupled with the ring oscillator, an oscillator cycle incrementing the counter, and the counter measuring cardinality of the plurality of oscillation cycles thereby.

41. The memory module of Claim 39, wherein the oscillation signal has alternating positive signal edges and negative

signal edges on successive ones of the plurality of oscillation cycles, and wherein the high-precision delay measurement circuit further comprises a positive edge counter and a negative edge counter, each of the positive edge counter and the negative edge counter measuring cardinality of the plurality of oscillation cycles.

42. The memory module of Claim 41, wherein the plurality of oscillation counters comprise a dual-edge detection counter.

43. The memory module of Claim 23, further comprising a high-precision delay measurement circuit constraining the limited voltage swing signal.

44. The memory module of Claim 43, wherein the high-precision delay measurement circuit comprises a ring oscillator executing oscillation cycle in a predefined oscillation period.

45. The memory module of Claim 44, wherein the ring oscillator executes a plurality of oscillation cycles by circulating an oscillation signal therein, and the ring oscillator comprises:

a. a plurality of oscillator stages; and

b. a plurality of oscillation signal detectors interposed between selected ones of the oscillator stages, the plurality of oscillation signal detectors detecting the location of the oscillation signal within the ring oscillator during a measured oscillation cycle, responsive to a measurement signal.

46. The memory module of Claim 45, wherein the high-precision delay measurement circuit further comprises a counter coupled with the ring oscillator, an oscillator cycle incrementing the counter, and the counter measuring cardinality of the plurality of oscillation cycles thereby.

47. The memory module of Claim 45, wherein the oscillation signal has alternating positive signal edges and negative signal edges on successive ones of the plurality of oscillation cycles, and wherein the high-precision delay measurement circuit further comprises a positive edge counter and a negative edge counter, each of the positive edge counter and the negative edge counter measuring cardinality of the plurality of oscillation cycles.

48. The memory module of Claim 47, wherein the plurality of oscillation counters comprise a dual-edge detection counter.

49. The memory module of Claim 23, further comprising a diffusion replica delay circuit constraining the limited voltage swing signal.

50. The memory module of Claim 49, wherein the diffusion replica delay circuit comprises dummy cells operably coupled with a selected wordline decoder and a selected sense amplifier.

51. The memory module of Claim 50, wherein the dummy cells comprise split dummy bit lines.

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52. The memory module of Claim 2, further comprising a data transfer bus circuit coupling the global sense amplifier to a data bus.

53. The memory module of Claim 52, wherein the data transfer bus circuit comprises a programmable driver, the programmable driver capable of imposing multilevel logic signals on the data bus.

54. The memory module of Claim 22, further comprising a data transfer bus circuit coupling a selected one of the pluralities of global sense amplifiers, local sense amplifiers, global wordline decoders, and local wordline decoders to a data bus, the circuit imposing a limited voltage swing on the data bus.

55. The memory module of Claim 54, wherein the data transfer bus circuit comprises a programmable driver programmed to impose logic signals on the data bus.

56. The memory module of Claim 55, wherein the programmable driver is programmed to impose encoded signals on the data bus.

57. The memory module of Claim 55, wherein the programmable driver is programmed to impose multilevel logic signals on the data bus.

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58. The memory module of Claim 22, wherein one of the pluralities of global sense amplifiers, local sense amplifiers, global wordline decoders, and local wordline decoders comprises a limited swing voltage circuit, the limited swing voltage circuit producing a limited swing

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voltage signal of a respective one of the global memory state signal, the local memory state signal, the global selection signal, the local selection signal.

59. The memory module of Claim 1, wherein the memory module is disposed in one of a semiconductor device, an optical device, and a combination thereof.

60. The memory module of Claim 1, wherein the memory module is embedded in a communication device.

61. The memory module of Claim 22, wherein the memory module is disposed in one of a semiconductor device, an optical device, and a combination thereof.

62. The memory module of Claim 22, wherein the memory module is embedded in a communication device.

~~61.~~ 63. The memory module of Claim 48, wherein the memory module is disposed in one of a semiconductor device, an optical device, and a combination thereof.

~~62.~~ 64. The memory module of Claim 48, wherein the memory module is embedded in a communication device.

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~~63.~~ 65. A hierarchical memory structure, comprising:

a. memory cells having respective memory states;

b. local sense amplifiers selectively coupled with the memory cells, selected ones of the local sense amplifiers sensing the respective memory states and producing respective local memory state signals representative thereof, wherein the local sense amplifiers produce limited swing voltage signals;

c. local wordline decoders selectively coupled with the memory cells, selected ones of the local wordline decoders selecting respective memory cells responsive to a corresponding local selection signal;

c. global sense amplifiers, selected ones of the global sense amplifiers being coupled with local sense amplifiers, selected ones of the local sense amplifiers being coupled with respective memory cells, selected others of the global sense amplifiers being coupled with the selected ones such that the selected ones of the global sense amplifiers are local sense amplifiers relative to the selected others of the global sense amplifiers in a multi-tiered hierarchy, each local sense amplifier producing a respective local memory state signal to which a corresponding global sense amplifier is responsive;

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d. global wordline decoders, selected ones of the global wordline decoders being coupled with respective local wordline decoders, selected others of the global wordline decoders being coupled with the selected ones such that the selected ones are local wordline decoders relative to the selected others in a multi-tiered hierarchy, each global wordline decoder producing a respective global selection signal to which corresponding local wordline decoders are responsive;

e. one of a single-ended sense amplifier having sample-and-hold reference, and a charge-share limited-swing-driver sense amplifier;

f. an asynchronously-resettable decoder;

g. a wordline decoder having a first memory row and a second memory row coupled therewith, the wordline decoder decoding the first memory row, and being

disposed to select and decode the second memory row responsive to an alternative-row-select signal;

h. with the memory module having a designated group of memory cells assigned to represent a logical portion of the memory structure, a redundancy device, including:

(1) a redundant group of memory cells; and

(2) a redundancy controller coupled with the designated group and the redundant group, the redundancy controller assigning the redundant group to the logical portion of the memory structure, responsive to a preselected memory group condition,

wherein each of the designated group and the redundant group comprises one of a memory row, a memory column, a preselected portion of a memory module, a selectable portion of a memory module, a memory module, and a combination thereof;

i. one of a diffusion replica delay circuit and a high-precision delay measurement circuit constraining a limited voltage swing signal; and

j. a data transfer bus circuit coupling a selected one of the global sense amplifiers, local sense amplifiers, global wordline decoders, and local wordline decoders to a data bus, the circuit imposing a limited voltage swing on the data bus.

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66. The memory module of Claim 62, wherein the hierarchical memory structure is disposed in one of a semiconductor device, an optical device, and a combination thereof.

67. The memory module of Claim 62, wherein the hierarchical memory structure is embedded in a communication device.

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65. A method for substantially simultaneously retrieving a first datum from a first memory location and storing a second datum in a second memory location, wherein both locations are disposed within a single-port hierarchical memory structure having local and global data sensing, and local and global location selecting, the method comprising:

a. locally selecting the first memory location from which the first datum is to be retrieved;

b. locally sensing the first datum (READ operation);

c. globally selecting the second memory location;

d. substantially concurrently with the globally selecting, globally sensing the first datum at the first memory location;

e. outputting the first data subsequent to the globally sensing;

f. inputting the second datum substantially immediately subsequent to the outputting the first datum;

g. locally selecting the second memory location; and

h. storing the second datum (WRITE operation).

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66. The method of Claim 65, further comprising precharging bitlines coupled with the first and the second memory locations, prior to locally sensing the first datum (PRECHARGE operation).

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67. The method of Claim 65, wherein (a) through (h) are completed within one access cycle of the memory structure.

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68. The method of Claim 66, wherein a plurality of PRECHARGE-READ-WRITE operations are completed within one access cycle of the memory structure.

~~69~~ 72. A method for providing sequential storage of a first datum in a first hierarchical memory structure location and a second datum in a second hierarchical memory structure location within one access cycle of the memory structure, the structure having local and global location selecting, the method comprising:

a. globally selecting the first hierarchical memory structure location to which the first datum is to be stored;

b. precharging bitlines coupled with the memory cells at the first hierarchical memory structure location (PRECHARGE1 operation);

c. locally selecting the first hierarchical memory structure location;

d. storing the first datum (WRITE1 operation);

e. globally selecting the second hierarchical memory structure location to which the second datum is to be stored;

f. substantially concurrently with the globally selecting the second hierarchical memory structure location, precharging bitlines coupled with the second hierarchical memory structure location (PRECHARGE2 operation);

g. locally selecting the second hierarchical memory structure location; and

h. storing the second datum (WRITE2 operation).

~~70~~ 73. A hierarchical memory structure comprising:

a. memory cells;

b. sense amplifiers coupled with the memory cells to form memory columns; and

c. decoders coupled with the memory cells to form memory rows,

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wherein the memory cells, sense amplifiers, and decoders so coupled form a first tier memory module, and at least one of the first tier sense amplifiers and the first tier decoders provide a limited swing voltage signal.

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71. The hierarchical memory structure of Claim 70, further comprising:

a. *(n-1)*-tier memory modules;

b. *(n)*-tier sense amplifiers coupled with the *(n-1)*-tier sense amplifiers in the *(n-1)*-tier memory modules; and

c. *(n)*-tier decoders coupled with the *(n-1)*-tier decoders in the *(n-1)*-tier memory modules,

wherein n > 1, and wherein the *(n-1)*-tier memory modules, *(n)*-tier sense amplifiers, and *(n)*-tier decoders so coupled form an *(n)*-tier memory module.

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72. The hierarchical memory structure of Claim 71, wherein one of the *(n)*-tier sense amplifiers, *(n-1)*-tier sense amplifiers, *(n)*-tier decoders, and *(n-1)*-tier decoders produces a limited swing voltage signal.

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73. The hierarchical memory structure of Claim 71, wherein one of the *(n)*-tier sense amplifiers, *(n-1)*-tier sense amplifiers, *(n)*-tier decoders, and *(n-1)*-tier decoders is responsive to a limited swing voltage signal.

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74. The hierarchical memory structure of Claim 72, wherein one of the *(n)*-tier sense amplifiers, *(n-1)*-tier sense amplifiers, *(n)*-tier decoders, and *(n-1)*-tier decoders is responsive to a limited swing voltage signal.

75. The hierarchical memory structure of Claim 70, wherein one of plurality of first tier decoders is an asynchronously resettable row decoder.

76. The hierarchical memory structure of Claim 70, further comprising one of a redundant memory row and a redundant memory column.

77. The hierarchical memory structure of Claim 71, wherein a selected one of the pluralities of *(n)*-tier sense amplifiers and *(n-1)*-tier sense amplifiers is one of a single-ended sense amplifier having sample-and-hold reference, and a charge-share limited-swing-driver sense amplifier.

78. The hierarchical memory structure of Claim 70, further comprising a row decoder having a first memory row and a second memory row coupled therewith, the row decoder decoding the first memory row, and being disposed to select and decode the second memory row responsive to an alternative-row-select signal.

79. The hierarchical memory structure of Claim 78, further comprising a row decoder having an assigned memory row and a redundant memory row coupled therewith, the row decoder decoding the assigned memory row, and being disposed to select and decode the redundant memory row responsive to a redundant-row-select signal.

80. The hierarchical memory structure of Claim 75, the asynchronously-resettable row decoder having a first memory row and a second memory row coupled therewith, the row decoder decoding the first memory row, and being

disposed to select and decode the second memory row responsive to an alternative-row-select signal.

81. The hierarchical memory structure of Claim 72, wherein one of the *(n)*-tier sense amplifiers and *(n-1)*-tier sense amplifiers is one of a single-ended sense amplifier having sample-and-hold reference, and a charge-share limited-swing-driver sense amplifier.

82. The hierarchical memory structure of Claim 81, wherein a second selected one of the pluralities of *(n)*-tier sense amplifiers, *(n-1)*-tier sense amplifiers, *(n)*-tier decoders, and *(n-1)*-tier decoders is responsive to a limited swing voltage signal.

83. The hierarchical memory structure of Claim 81, wherein one of the decoders is an asynchronously resettable row decoder.

84. The hierarchical memory structure of Claim 83, further comprising a row decoder having a first memory row and a second memory row coupled therewith, the row decoder decoding the first memory row, and being disposed to select and decode the second memory row responsive to an alternative-row-select signal.

85. The hierarchical memory structure of Claim 83, wherein the asynchronously-resettable row decoder is coupled with a first memory row and a second memory row, the row decoder decoding the first memory row, and being disposed to select and decode the second memory row responsive to an alternative-row-select signal.

86. The hierarchical memory structure of Claim 83, further comprising one of a redundant memory row and a redundant memory column.

87. The hierarchical memory structure of Claim 86, further comprising a row decoder having an assigned memory row and a redundant memory row coupled therewith, the row decoder decoding the assigned memory row, and being disposed to select and decode the redundant memory row responsive to a redundant-row-select signal.

88. The hierarchical memory structure of Claim 71, having a designated group of memory cells assigned to represent a logical portion of the memory structure, the structure further comprising:

a. a redundant group of memory cells; and

b. a redundancy controller coupled with the designated group and the redundant group, the redundancy controller assigning the redundant group to the logical portion of the memory structure, responsive to a preselected memory group condition.

89. The hierarchical memory structure of Claim 88, wherein the redundancy controller comprises a redundancy decoder responsive to an encoded signal representative of the preselected memory group condition.

90. The hierarchical memory structure of Claim 89, wherein the redundancy controller further comprises a plurality of selectable switches, the plurality of selectable switches encoding the preselected memory group condition.

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91. The hierarchical memory structure of Claim 90, wherein the plurality of selectable switches are fuses.

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92. The hierarchical memory structure of Claim 90, wherein the preselected memory group condition is a "FAILED" memory group condition, representative of a designated group malfunction.

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93. The hierarchical memory structure of Claim 88, wherein each of the designated group and the redundant group comprise one of a memory row, a memory column, a preselected portion of a memory module, a selectable portion of a memory module, a memory module, and a combination thereof.

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94. The hierarchical memory structure of Claim 72, further comprising a limited swing voltage driver circuit constraining the limited swing voltage signal.

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95. The hierarchical memory structure of Claim 72, further comprising a high-precision delay measurement circuit constraining the limited swing voltage signal.

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96. The hierarchical memory structure of Claim 95, wherein the high-precision delay measurement circuit comprises a ring oscillator executing oscillation cycle in a predefined oscillation period.

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97. The hierarchical memory structure of Claim 96, wherein the ring oscillator executes a plurality of oscillation cycles by circulating an oscillation signal therein, and the ring oscillator comprises:

a. a plurality of oscillator stages; and

b. a plurality of oscillation signal detectors interposed between selected ones of the oscillator stages, the plurality of oscillation signal detectors detecting the location of the oscillation signal within the ring oscillator during a measured oscillation cycle, responsive to a measurement signal.

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~~98~~. The hierarchical memory structure of Claim 97, wherein the high-precision delay measurement circuit further comprises a counter coupled with the ring oscillator, an oscillator cycle incrementing the counter, and the counter measuring cardinality of the plurality of oscillation cycles thereby.

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~~99~~. The hierarchical memory structure of Claim 98, wherein the oscillation signal has alternating positive signal edges and negative signal edges on successive ones of the plurality of oscillation cycles, and wherein the high-precision delay measurement circuit further comprises a positive edge counter and a negative edge counter, each of the positive edge counter and the negative edge counter measuring cardinality of the plurality of oscillation cycles.

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~~100~~. The hierarchical memory structure of Claim 99, wherein the plurality of oscillation counters comprise a dual-edge detection counter.

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~~101~~. The hierarchical memory structure of Claim 72, further comprising a diffusion replica delay circuit constraining the limited voltage swing signal.

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~~102~~. The hierarchical memory structure of Claim 101, wherein the diffusion replica delay circuit comprises dummy cells

operably coupled with a selected wordline decoder and a selected sense amplifier.

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~~103~~. The hierarchical memory structure of Claim 102, wherein the dummy cells comprise split dummy bit lines.

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~~104~~. The hierarchical memory structure of Claim 71, further comprising a data transfer bus circuit coupling a selected one of the pluralities of global sense amplifiers, local sense amplifiers, global wordline decoders, and local wordline decoders to a data bus, the circuit imposed a limited voltage swing on the data bus.

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~~105~~. The hierarchical memory structure of Claim 104, wherein the data transfer bus circuit comprises a programmable driver programmed to impose logic signals on the data bus.

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~~106~~. The hierarchical memory structure of Claim 105, wherein the programmable driver is programmed to impose encoded signals on the data bus.

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~~107~~. The hierarchical memory structure of Claim 105, wherein the programmable driver is programmed to impose multilevel logic signals on the data bus.

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